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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,683	10/14/2003	Dikran Babikian	006601P034C	7073

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EXAMINER	
FRANK, ELLIOT L	

ART UNIT	PAPER NUMBER
2125	

DATE MAILED: 09/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,683	BABIKIAN ET AL.	
	Examiner	Art Unit	
	Elliot L Frank	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,17-21,23 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,17-21,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/14/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Claims 13-16,22,25 and 26 have been cancelled by preliminary amendment leaving claims 1-12,17-21,23 and 24 pending in the instant application.
2. This application is a continuation of application 09/602,527, which is a CIP of 09/336,275 that claims priority to provisional 60/114,442 filed 31 December 1998 and provisional 60/140,661 filed 23 June 1999.

   09/336,275 has been reviewed in relation to claims 1-12,17-21,23 and 24. Support for claims 1-12 was not found in the specification for 09/336,275. Therefore, the priority date for claims 1-12 has been established at 23 June 1999. The priority date for the balance of the claims is 31 December 1998.
3. Claims 1-12,17-21,23 and 24 have been considered and are deemed identical to the original claims as filed in the parent application 09/602,527.

Specification

4. The specification has been considered and is deemed identical to the parent application. These objections have been made in view of this similarity.
5. The disclosure is objected to because of the following informalities:
   a. The item numbers in the specification that reference specific parts of the drawing figures are not delineated in a clear manner. The applicant is requested to punctuate the indicated drawing item

numbers so that they can be easily read. Some examples are page 13, line 9: "104,106,108", line 17: "wafer 1, 208,", etc.

b. The drawings submitted by the applicant corrected a duplicate numbering problem, indicated in the parent application, by changing the "chart" reference from "818" to "816" in figure 8 and updating the specification accordingly in the paragraph starting on page 25, line 11. The specification in the instant application requires a correction to follow the cited changes in the drawings.

c. Any correction made on the applicant's own volition in the parent application 09/602,527 should be applied to the instant application.

Appropriate correction is required.

Claim Objections

6. Claims 8 and 17 are objected to because of the following informalities:

d. The word "software" should be inserted after the word "timetable" in line 1 of claim 8 to preserve the uniformity of the claim language.

e. The word "model" in line 17 should be corrected to "module".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to

be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (USPN 6,298,274 B1) in view of Jevtic (5,928,389 A).

Inoue, a semiconductor wafer transport system, does not specify a cluster tool process format, however, it does read on the functionality of the following claims with regard to wafer transport:

1. A plurality of processing stations for processing wafers (column 1, lines 34-52), each processing station further comprising

a process chamber (column 1, lines 23-33),

a local clock coupled to the process chamber (column 4, lines 58-60);

a master server in communication with the local clock in each processing station (column 3, lines 57-61), the master server including

a master clock (it was well known in the art at the time the invention was made that a computer as described at column 3, lines 57-61, would contain a clock that would dictate the passage of time on the master system).

2. The wafer cluster tool of claim 1, wherein each processing station further comprises:

a CPU coupled to the processing station, wherein the local clock coupled to the process chamber resides on the CPU (column 4, lines 8-60);

3. The wafer cluster tool of claim 2 further comprising: a local area network, wherein the master server is coupled to the CPU in each processing station via the local area network (column 3, lines 57-61).

4. The wafer cluster tool of claim 3, further comprising: a CPU coupled to the master server, wherein the master clock is resident on the CPU coupled to the master server (it was well known in the art at the time the invention was made that a computer as described at column 3, lines 57-61, would contain a clock that would dictate the passage of time on the master system).

Inoue does not read on the requirements of claims 1-5 for a cluster manufacturing system or a relational database for storing timetable information.

Jevtic, analogous to Inoue in that both are semiconductor wafer transport systems (Jevtic, column 1, lines 9-13), reads on the additional limitations of claims 1-5 at column 1, lines 15-25, wherein it describes the cluster tool configuration as a well known modular tool that provided multiple sequential process steps for semiconductor manufacturing at the time the invention was made, and at column 9, lines 31-66, wherein it describes a relational database system for storing the start and end times of semiconductor wafer processes.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the functionality of Jevtic into Inoue to have created an improved scheduling routine to increase throughput of a cluster tool (Jevtic, column 6, lines 7-9).

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (USPN 6,298,274 B1) in view of Jevtic (5,928,389 A) as applied to claim 1 above, and further in view of Nulman (USPN 6,408,220 B1).

Claim 6 depends from Claim 1. Claim 1 has been shown to be obvious in view of the combination of Inoue and Jevtic.

The aforementioned combination does not read on the additional limitations of claim 6:

6. The wafer cluster tool of claim 1, wherein the master server is coupled to the CPU in each processing; station via the Internet.

Nulman, analogous to the combination of Inoue and Jevtic in that all three systems are applicable to semiconductor processing (Nulman, column 1, lines 14-15), reads on the additional requirements of claim 6 at column 18, lines 62-67 wherein it describes the internet as a communication means in a semiconductor manufacturing system.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the functionality of Nulman into the aforementioned combination to have allowed for remote database or management functions (Nulman, column 18, lines 62-67).

10. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (USPN 6,298,274 B1) in view of Jevtic (5,928,389 A) as applied to claim 1 above, and further in view of Baker et al. (USPN 5,226,118 A).

Claims 7 and 8 depends from Claim 1. Claim 1 has been shown to be obvious in view of the combination of Inoue and Jevtic.

The aforementioned combination does not read on the additional limitations of claims 7 and 8:

7. The wafer cluster tool of claim 1, wherein the timetable software comprises a spreadsheet.

8. The wafer cluster tool of claim 7, wherein the timetable is updated in real-time.

Baker et al., analogous to the combination of Inoue and Jevtic in that all three systems are applicable to semiconductor processing (Baker et al., column 1, lines 49-53), reads on the additional requirements of claims 7 and 8 at column 3, lines 28-39 wherein it describes the use of spreadsheets for real time data gathering.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the functionality of Baker et al. into the aforementioned combination to have made it easier to collect analysis data from a wide variety of systems (Baker et al., column 3, lines 1-9).

11. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (USPN 6,298,274 B1) in view of Jevtic (5,928,389 A) as applied to claim 1 above, and further in view of Yokoyama et al. (USPN 5,858,863 A).

Claims 9-12 depends from Claim 1. Claim 1 has been shown to be obvious in view of the combination of Inoue and Jevtic.

The aforementioned combination does not read on the additional limitations of claims 9-12:

9. The wafer cluster tool of claim 1, wherein the master server further includes scheduling software for the cluster tool.

10. The wafer cluster tool of claim 9, wherein the scheduling software includes a pre-determined schedule for the cluster tool.

11. The wafer cluster tool of claim 10, wherein the pre-determined schedule is periodic according to a fixed sending period.

12. The wafer cluster tool of claim 11, wherein the time recorded on the local clocks of each processing station is measured in units of the sending period.

Yokoyama et al., analogous to the combination of Inoue and Jevtic in that all three systems are applicable to semiconductor processing (Yokoyama et al., column 1, lines 12-14), reads on the additional requirements of claims 9-12 as follows:

9. The wafer cluster tool of claim 1, wherein the master server further includes scheduling software for the cluster tool (column 6, line 66-column 7, line 21).

10. The wafer cluster tool of claim 9, wherein the scheduling software includes a pre-determined schedule for the cluster tool (see example of pre-planned process at column 12, line 62-column 13, line 10).

11. The wafer cluster tool of claim 10, wherein the pre-determined schedule is periodic according to a fixed sending period (column 9, line 64-column 10, line 6).

12. The wafer cluster tool of claim 11, wherein the time recorded on the local clocks of each processing station is measured in units of the sending period (column 10, lines 26-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the functionality of Yokoyama et al. into the aforementioned combination to have made a processing system that was capable of shortening the term of a sequence of processes applied to works while making efficient use of processing apparatus (Yokoyama et al., column 6, lines 1-13).

12. Claims 17-21, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokoyama et al. (USPN 5,858,863 A) in view of Jevtic (5,928,389 A).

Claims 17 through 19 describe a process wherein three wafers are transferred between four cluster modules in one period of time by a robot transfer arm. Wafer 1 is loaded into the cluster tool, Wafer 2 is moved from chamber 1 to chamber 2 and wafer 3 is moved from chamber 3 to chamber 4. in each move, the arm is moved to the next pickup location immediately. Claim 23 requires that the system modules be interconnected by a network, and claim 24 requires that the arm have only one gripper.

Yokoyama reads on the requirements of claims 17-19 at column 14, line 47 to column 15 line 3, and the process is shown in figure 4. Within one period multiple wafers are moved from the last position, which can be a chamber or a loading position, to the next position by a robot arm (figure 2). The limitations of claim 23 can be found at column 7, lines 10-13 and claim 24 is a single gripper robot device as depicted in figure 2.

Yokoyama does not read on the requirement that the arm be moved immediately to the next pick-up location via an algorithm or linear program.

Jevtic, analogous to Yokoyama in that both are semiconductor wafer movement systems (Jevtic, column 1, lines 9-13), reads on the additional limitations of the aforementioned claims at column 7 line 59-column 8, line 16, wherein it describes a process of immediately moving the robot to the scheduled next pick-up position and waiting for the wafer to finish processing.

Jevtic also makes obvious the requirements of claims 20 and 21 at column 2, line 62-column 3, line 27 wherein a scheduling algorithm to optimize the process throughput of the tool is demonstrated as well known in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the functionality of Jevtic into Yokoyama et al. to have created an improved scheduling routine to increase throughput of a cluster tool (Jevtic, column 6, lines 7-9).

13. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject

matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

USPN 6,099,598 A – Yokoyama et al. – Semiconductor process control

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elliot L Frank whose telephone number is (703) 305-5442. The examiner can normally be reached on M-F 7-4:30, 1st Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P Picard can be reached on (703) 308-0538. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ELF
23 August 2004

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